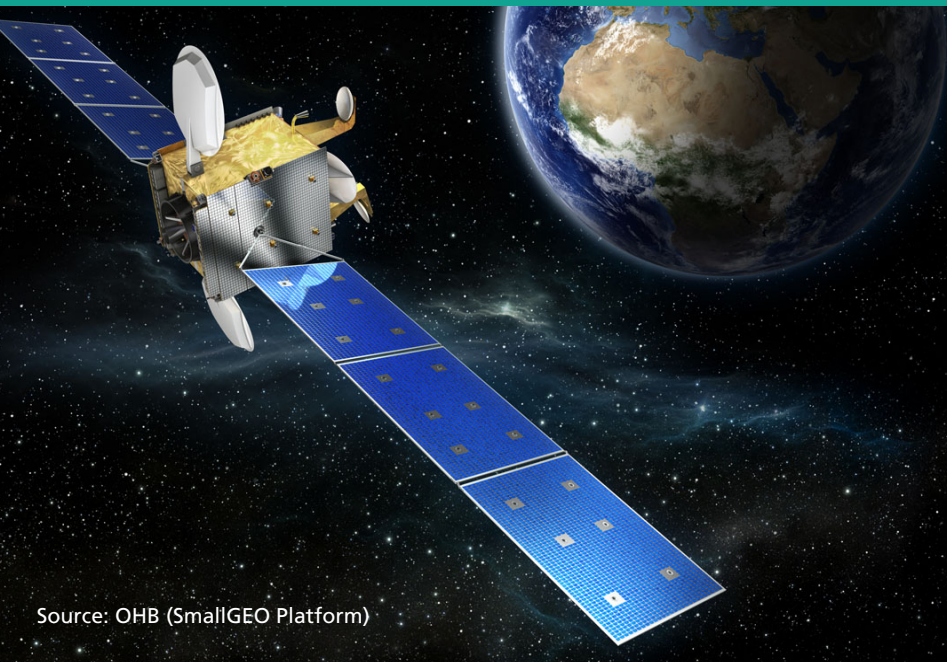# FPGA-BASED BROADBAND PROCESSING IN SPACE
(FRAUNHOFER ON-BOARD PROCESSOR)

Wireless Innovation Forum European Conference

Robért Glein, November 6th, 2014

Fraunhofer Institute for Integrated Circuits, Germany
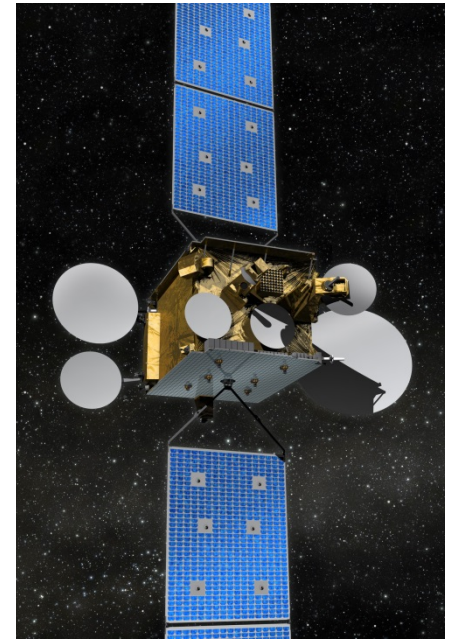
Source: OHB (SmallGEO Platform)

Source: Xilinx

OUTLINE

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Introduction
Heinrich Hertz Satellite Mission

Source: OHB

- First German communication satellite since ~25 years

- SmallGEO platform developed by OHB

- ~50 % **scientific** (experimental) payload

- ~50 % military payload

- Satellite will be launched in **2018/2019**

  - *Geostationary Earth Orbit* (GEO)

  - Most probably at 17.6 ° East

- Satellite life time of 15 years planned

- Scientific/technical experiments

  - In-Orbit-Verification

  - **Fraunhofer On-Board Processor (FOBP)**
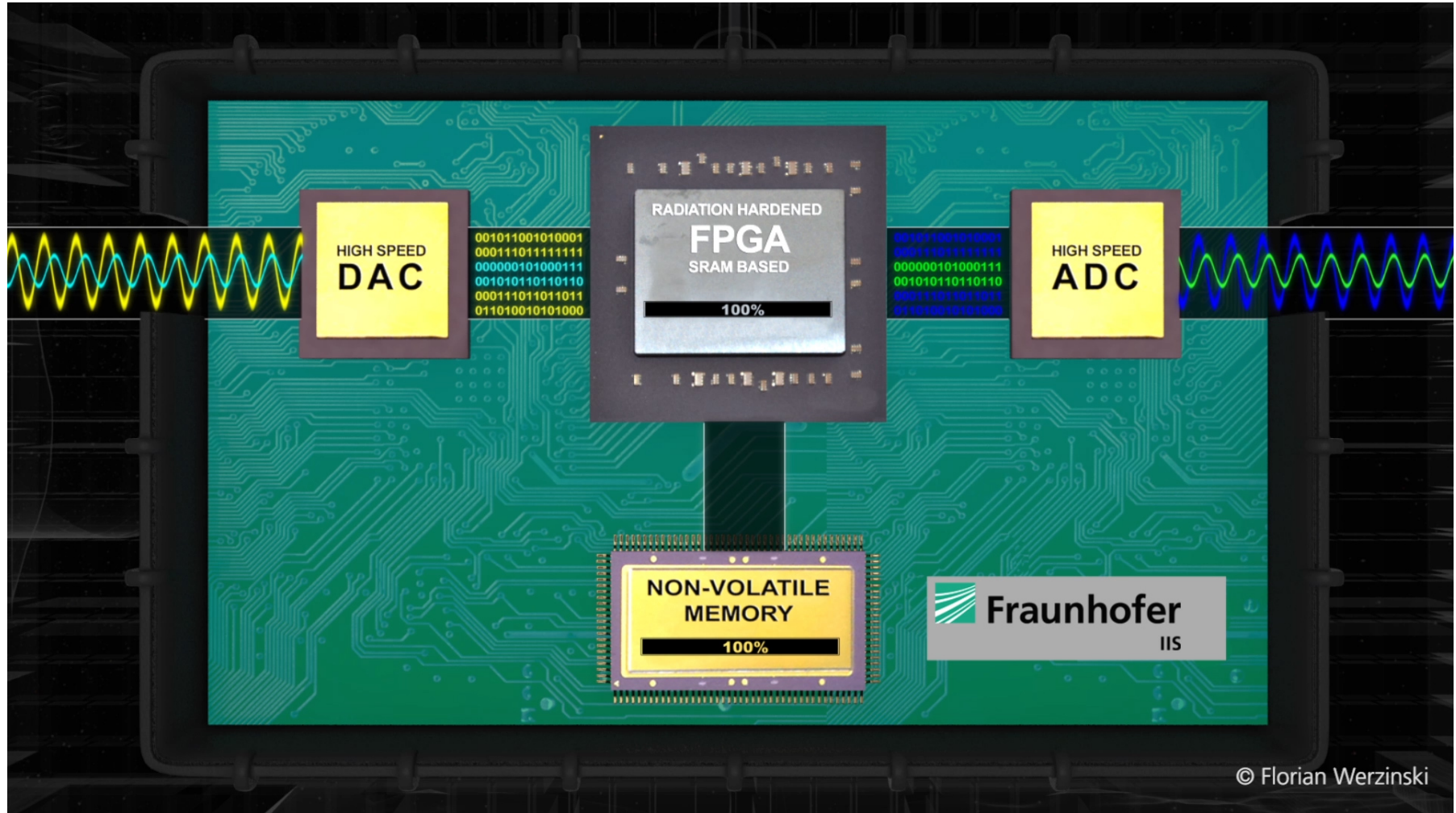
Total mass:	3.2t
Payload mass:	400 kg
Power:	3.6 kW

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Introduction: FOBP on the Heinrich Hertz Satellite
https://www.youtube.com/watch?v=6duxZbBJJeU
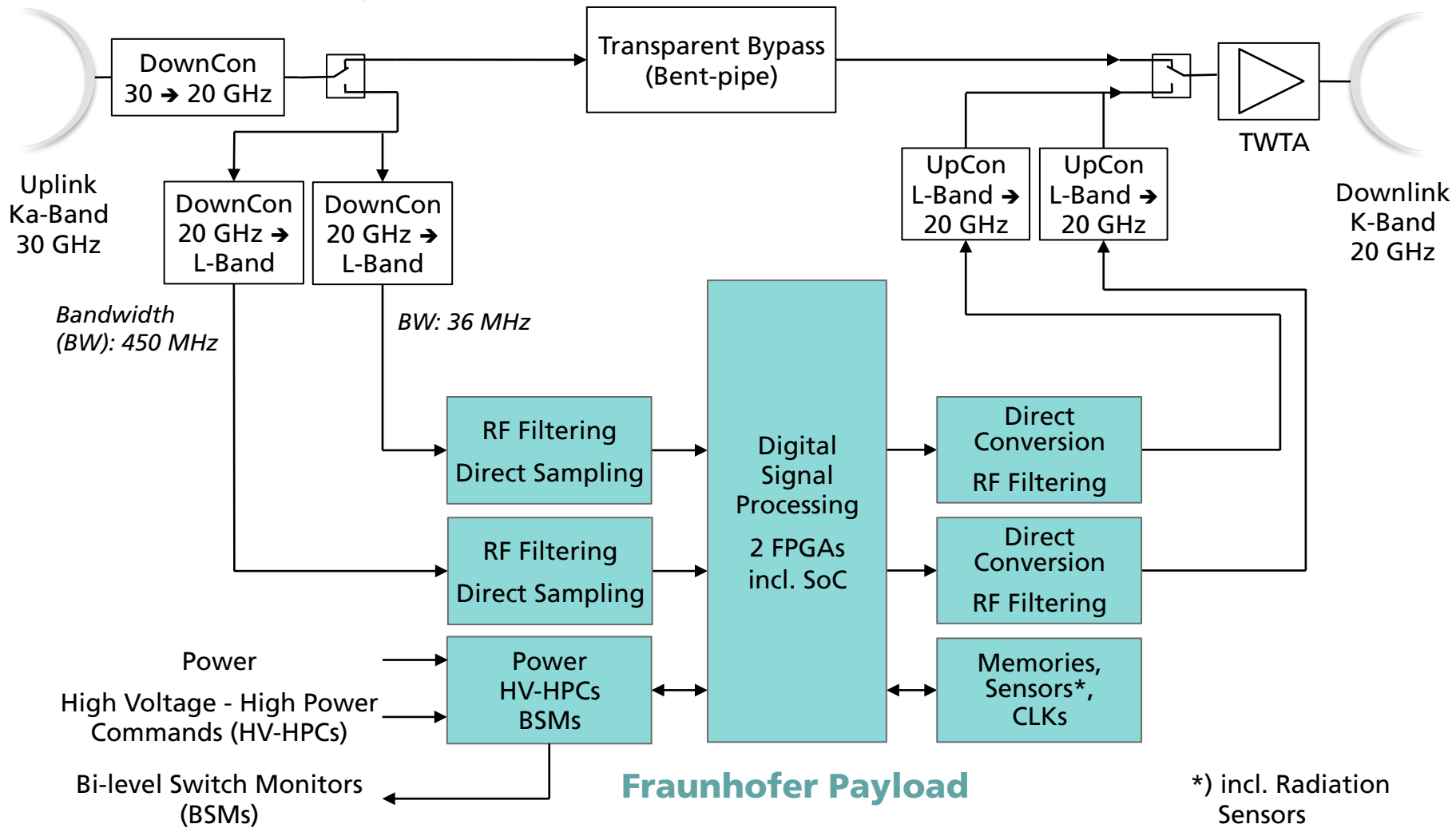

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Introduction
Advantages and new opportunities of using an OBP

- Ability of On-Board signal processing:

  - **Error correction** on half of the communication link leads to an increase of system performance (higher SNR):
    ➔ Higher modulation schemes which results in higher data rates
    ➔ Decrease of transmit power and lower power consumption with leads to increase of the stand-by times
    ➔ Decrease of the antenna aperture of mobile devices (smaller devices possible)

  - **Digital filtering:** Accurate selection of the band (FDMA)

  - **Automatic Gain Control** (AGC) -> Adjustment / perfect matching of the Analog-to-digital converters dynamic range

- **On-Board Routing:** Single-Hop-Connection w/o any Hub-Station (half of the latency)

- <u>**Reconfigurable OBP**</u>**: Flexibility for future communication standards**
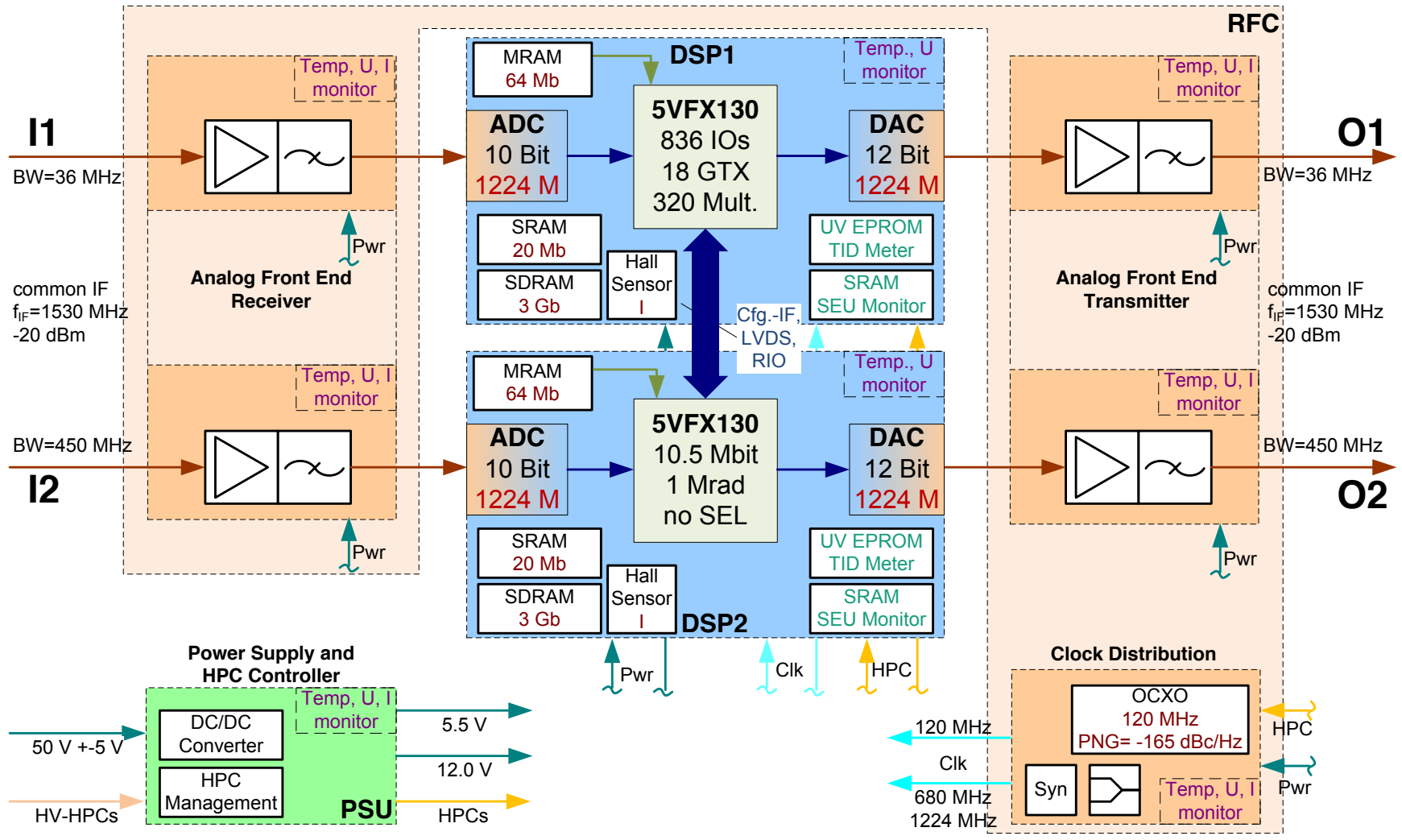
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Fraunhofer On-Board Processor (FOBP)
Fraunhofer Payload

Uplink
Ka-Band
30 GHz

| DownCon 30 → 20 GHz |
| Transparent Bypass (Bent-pipe) |
| TWTA |

Downlink
K-Band
20 GHz

| DownCon 20 GHz → L-Band |
| DownCon 20 GHz → L-Band |

Bandwidth (BW): 450 MHz

BW: 36 MHz

| UpCon L-Band → 20 GHz |
| UpCon L-Band → 20 GHz |

RF Filtering
Direct Sampling

Digital
Signal
Processing

2 FPGAs
incl. SoC

Direct
Conversion
RF Filtering

RF Filtering
Direct Sampling

Direct
Conversion
RF Filtering

Power

High Voltage - High Power
Commands (HV-HPCs)

Power
HV-HPCs
BSMs

Memories,
Sensors*,
CLKs

Bi-level Switch Monitors
(BSMs)

Fraunhofer Payload

*) incl. Radiation
Sensors

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Fraunhofer On-Board Processor (FOBP)
Block Diagram

Fraunhofer On-Board Processor (FOBP)
SDR Capabilities: Constraints

- Constraints because of space grade components
    - High power consumption
    - High reliability
- SDR performance is mainly limited by:
    - Filter, ADC and DAC
    - FPGA
    - OCXO (Oven Controlled Crystal Oscillator) and synthesizer
- Following filter are not considered (application specific)
    - FOBP filter:
        - Low pass (LC) at the input (channel is already filtered by the satellite)
        - Band pass SAW (Surface Acoustic Wave) filter for the output

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Fraunhofer On-Board Processor (FOBP)
SDR Capabilities: Important Parameter

Parameter	Value	Limited by	Comment	FOBP
Analog f_{in}	1...**2250** MHz	ADC	1.-3. (-5.) Nyquist	1530 MHz
NPR*	**43** dB	ADC	10 Bit ADC	10 Bit
Input BW	5...750 MHz	Synth., ADC		612 MHz
Processing BW	0...**612** MHz	FPGA	Quad muxed IF	612 MHz
Output BW	5...1500 MHz	Synth., DAC		612 MHz
NPR*	45 dB	DAC	12 Bit DAC	12 Bit
Analog f_{out}	1...6000 MHz	DAC	1.-5. Nyquist (different modes)	1530 MHz
Clock PNG*	-165 dBc/Hz @100 kHz	OXCO	120 MHz	$f_{clk}=$ 120 MHz
Sampling PNG*	**-160 dBc/Hz @100 kHz**	Synthesizer	5...3000 MHz	$f_{s}=$ 1224 MHz

* Parameter specified for a specific operating point or range;   NPR: Noise Power Ratio,
BW: Bandwidth, IF: Interface, PNG: Phase Noise Ground, OXCO: Oven Controlled Crystal Oscillator, f_s: Sampling frequency

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Fraunhofer On-Board Processor (FOBP)
Development Progress

- *Elegant Bread Board* (EBB)
    - Currently used for proof of concept
    - Backplane-based rack system
- *Engineering Model* (EM)
    - Currently under design
    - Use the Virtex5-QV and EM parts
    - Frontplane-based card system
    - Available at Q2 2015
    - 368x181x248 mm³, ~16 kg, ~161 W
- *Engineering Qualification Model* (EQM)
- *Proto-Flight Model* (PFM)

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Fraunhofer On-Board Processor (FOBP)
Central Component: FPGA XQR5V

- FPGA Virtex-5QV, radiation-hard space qualified, ITAR license required
- TID (Total Ionizing Dose) at least 1000 krad (Si)
- **SEL (Single-Event Latch-up) immune** and SEU (SE upsets) radiation-hard
- Hardened Components
    - Configuration: 12T Config. Memory; TMR Configuration Controller
    - CLB: 12T Latches; SET Filter Option
    - IOB: 12T Latches; TMR DCI Block
    - BRAM: EDAC Write Back Option
- Not Hardened Components
    - DSP, DCM, PLL, MGT (PCIe, EMAC, …)

- 65 nm Cu-CMOS
- 1752 Pins, 836 I/Os
- 1.0 V (10 A, Core)
- 42.5 mm x 42.5 mm

- 320 DSP48 (25x18 Multiplier)
- 20,480 Slices (4xLUT, 4xFF)
- 11 Mb BRAM
- ...

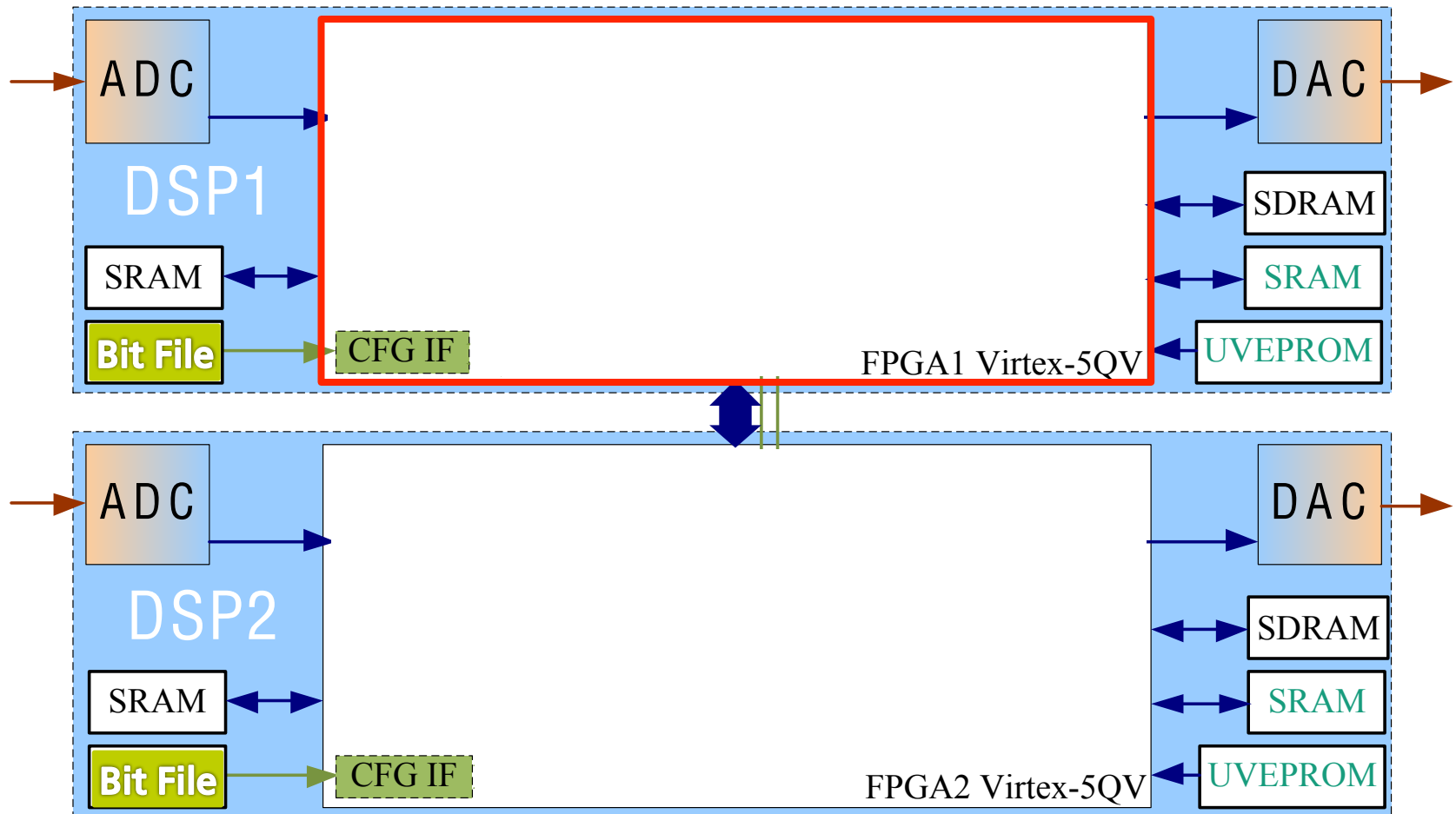TMR: Triple Modular Redundancy, CLB: Configurable Logic Block, BRAM: Block RAM, DSP48 Slice: Digital Multiplier
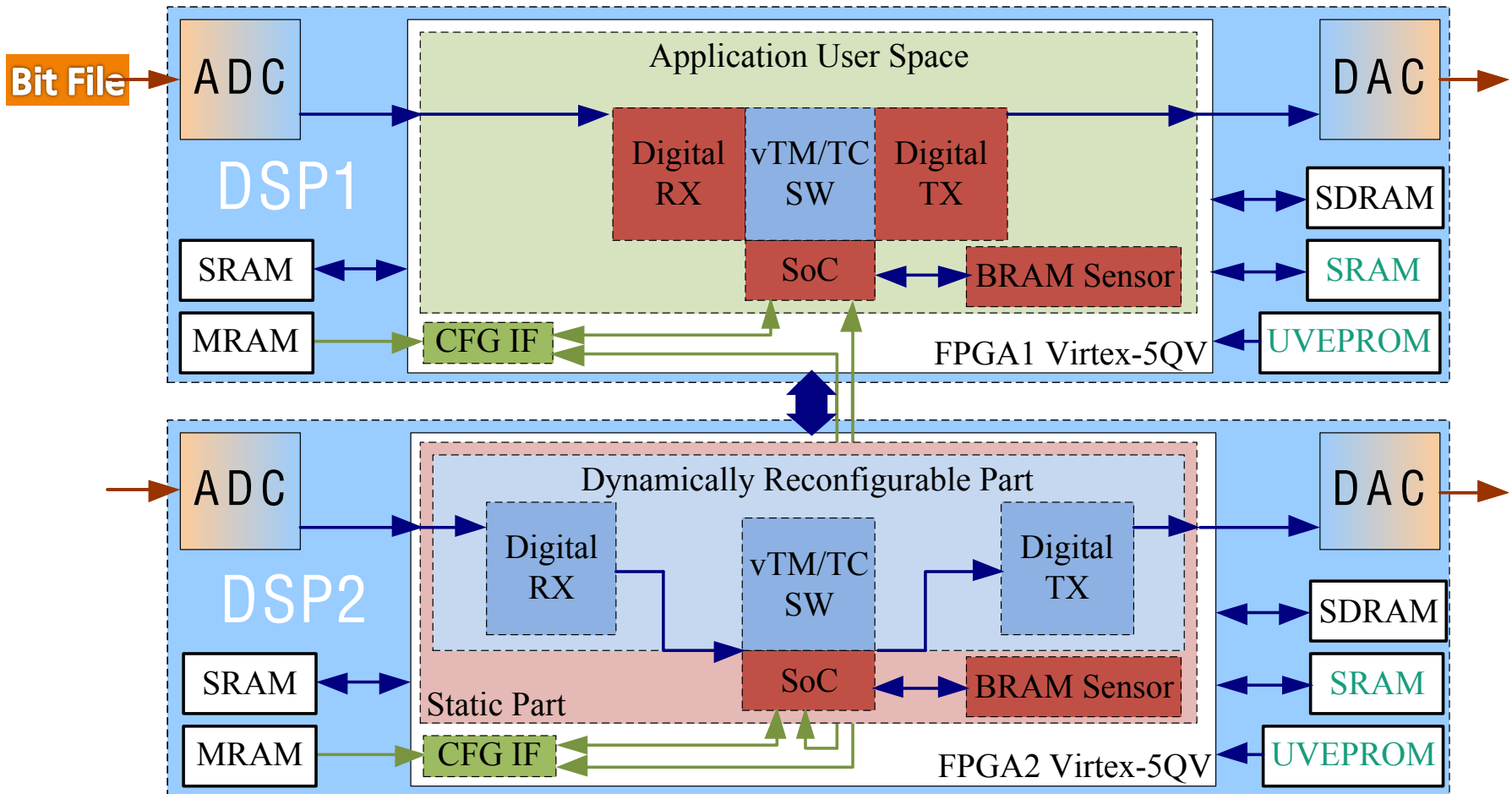
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Reliable Remote FPGA Reconfiguration [1]
FOBP Initial State and Master Determination
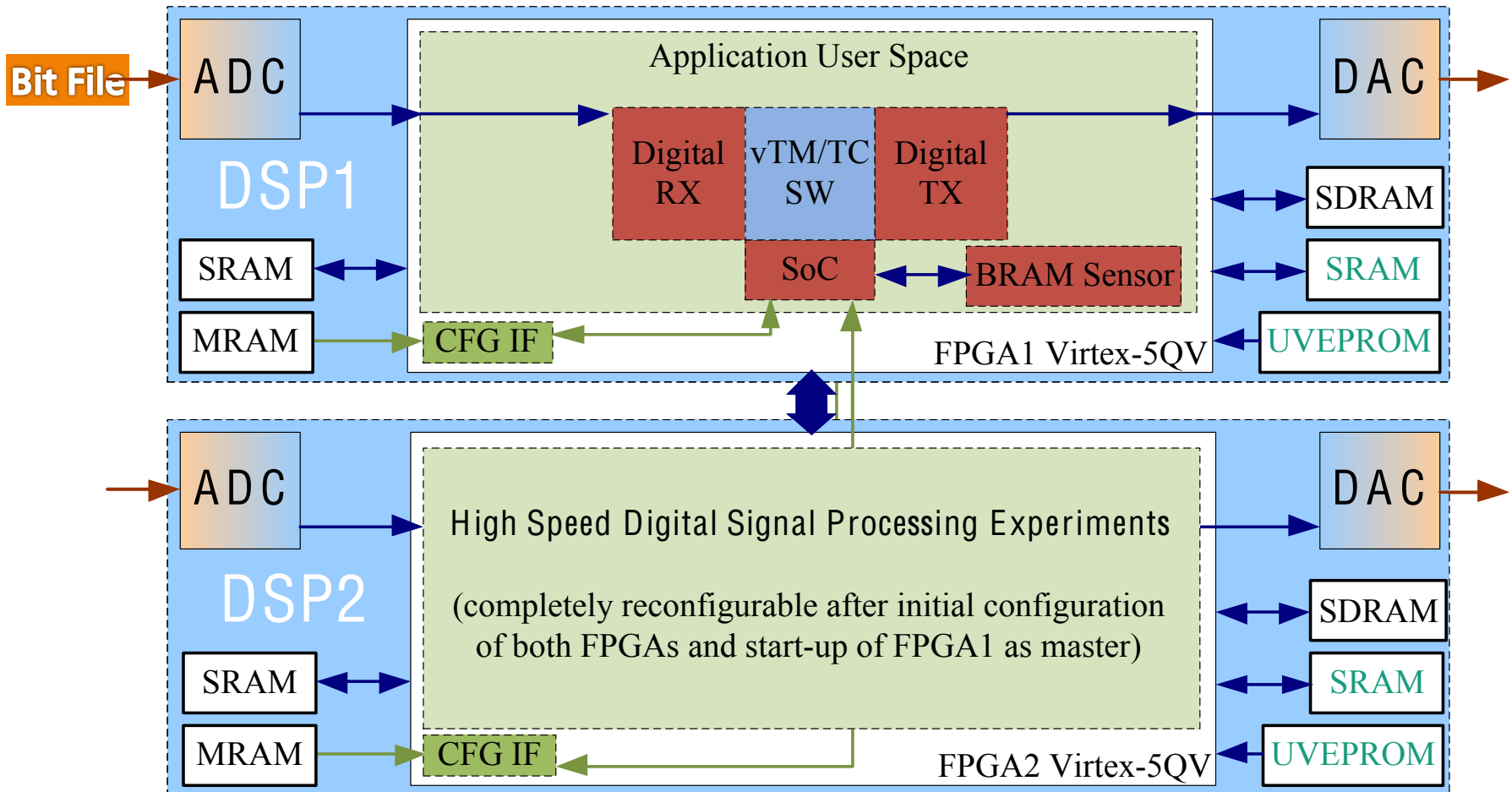
Reliable Remote FPGA Reconfiguration
Master FPGA Reconfiguration (FOBP Control Part)

Reliable Remote FPGA Reconfiguration
Slave FPGA Reconfiguration (Broadband DSP Part)

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Reliable Remote FPGA Reconfiguration
Reliability for FPGA Reconfiguration (15 years, GEO)

- SOTA configuration (by an external FPGA / ASIC / Microprocessor)

  - Depends on external configurator, memory, periphery, PCB, …

  - FIT rate = 1000 (assumption, typical value)

  - Results in a reliability of R_{RC}=87.7 %

- Initial fail-safe configuration via partial reconfiguration (static overhead)

  - Depends only on the MRAM

  - FIT rate = 100 (assumption, typical value)

  $$R(t) = e^{-\lambda t}$$

  - Results in a reliability of R_{FC}=98.7 %

- Parallel use of both

  $$R_{parallel}(t) = 1 - \prod_{i=1}^{n}(1 - R_i(t))$$

  - **Eliminates the SPOF** and enables whole FPGA reconfiguration

  - Results in a reliability of $R_{parallel}$= 99.8 % → **increase by 12.1 %**

SOTA: State-of-the-art, FIT: Failure in Time [failure / 10^9 h], SPOF: Single Point of Failure

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Adaptive Mitigation
Problem: Single Event Effects (SEEs) in SRAM based FPGAs

- SEL (Single Event Latch-up) immune

- SEFI (Single Event Functional Interrupt)

- **SEU (Single Event Upset)**
  - SEU CFG (configuration)

- SET (Single Event Transient)

Logic Layer

Routing Layer

Configuration Layer (SRAM)

Buffers and Package

Measure BRAM SEU Rate

SEU BRAM

SET

SEU

SEU CFG

Apply Mitigation Scheme

Cfg-Ctrl

SEFI

Heavy Ions and High Energy Protons

- **Resource consumption** of mitigation schemes such as
  - N-times Modular Redundancy (NMR: DMR or DWC, TMR, …)
  - Algorithm-Based Fault Tolerance (ABFT), …

- → Goal: **Adaptive Mitigation** (only use redundancy when needed)

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Adaptive Mitigation
Radiation Analysis Concept

- **How to mitigate SEUs?**
  - *Hardening by Technology* → fabrication process (*Silicon on Insulator*)
  - *Hardening by Design*
  - *Hardening by System* } TMR, EDAC

- **How to evaluate a firmware design according to SEUs?**
  - Device characterization → from manufacture (*Weibull* parameter)
  - Orbit characterization → CREME96 tool
  - SEU rate determination → calculation for the implemented design

TMR: Triple Modular Redundancy, EDAC: Error Detection and Correction

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Adaptive Mitigation
Virtex-5QV FPGA SEU Rate

"Flare" enhanced condition

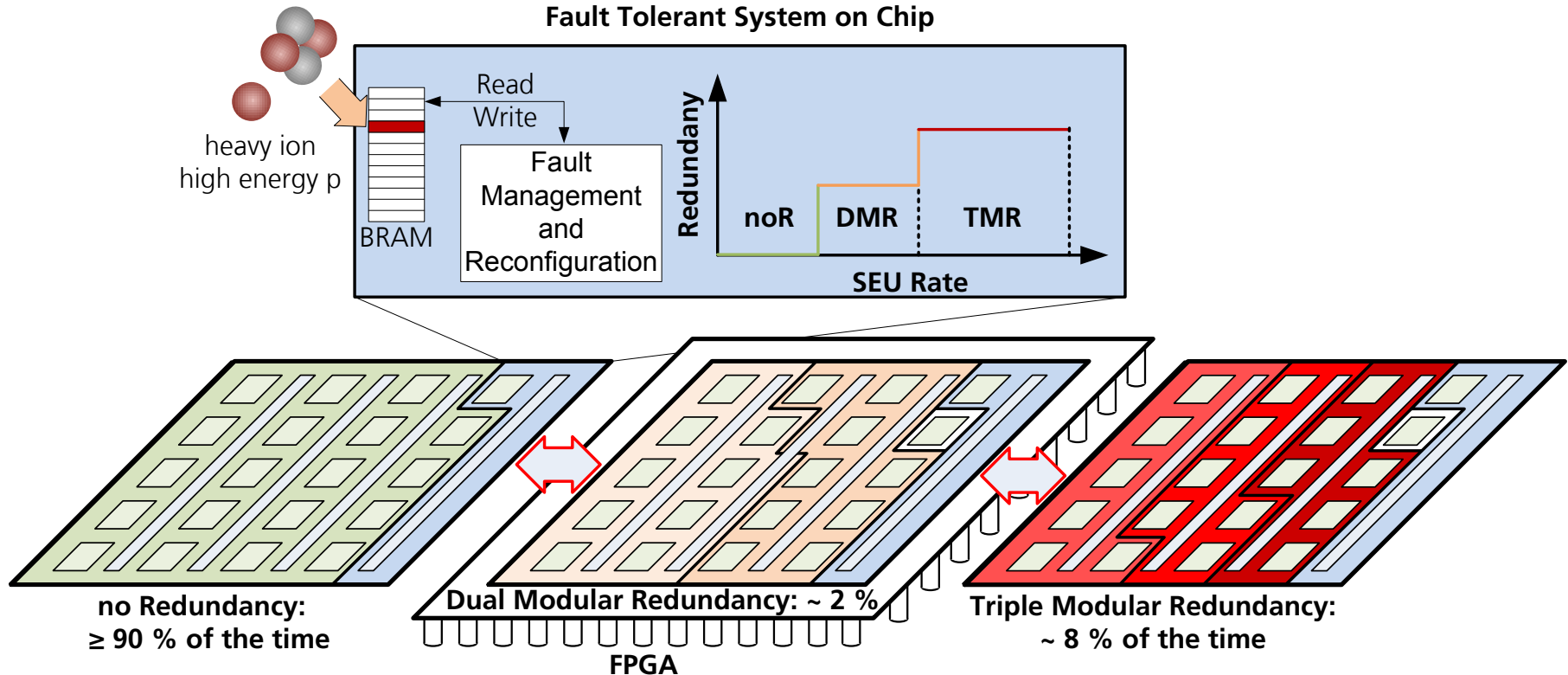| Solar Condition / Virtex-5QV	Solar-Minimum Upset/day/device	Solar-Maximum Upset/day/device	Worst-Week Upset/day/device	Worst-Day Upset/day/device	Peak-5 Upset/day/device
CFG Contoller (TMR + Voter; SEFI)	6.167E-07	1.728E-07	6.777E-05	2.542E-04	9.279E-04
CFG Memory (SEU CFG)	1.743E-03	3.007E-04	1.149E-01	3.282E-01	1.185E+00
BRAM (Block Memory Bits)	3.968E+00	1.248E+00	4.460E+02	1.837E+03	6.743E+03
FF (Transient filter off)	3.826E-03	9.188E-04	3.056E-01	1.070E+00	3.900E+00
FF (Transient filter on)	2.734E-02	6.426E-03	1.329E+00	4.130E+00	1.501E+01
DSP (M-REG)	1.268E-01	4.497E-02	1.196E+02	4.699E+02	1.713E+03
DSP (other)	2.801E-01	9.921E-02	2.618E+02	1.027E+03	3.746E+03

Overall upset rates μ of the Virtex-5QV in GEO with 4.5 mm AL shielding

- BRAM will be mitigated via ECC

- FFs and DSPs criticality depends highly on the design (feedback, filter, …)

- Analysis for CMTs, MGTs and IOBs available

ECC: Error Correction Code, DSP: 25x18 bit Multiplier, CMT: Clock Management Tile, MGT: Multi Gigabit Transceiver, IOB: Input Output Buffer

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Adaptive Mitigation [2]
Optimal Redundancy at Runtime in Cognitive Radio

Fault Tolerant System on Chip

heavy ion
high energy p

BRAM

Read
Write

Fault
Management
and
Reconfiguration

Redundany

noR   DMR   TMR

SEU Rate

no Redundancy:
≥ 90 % of the time

Dual Modular Redundancy: ~ 2 %

FPGA

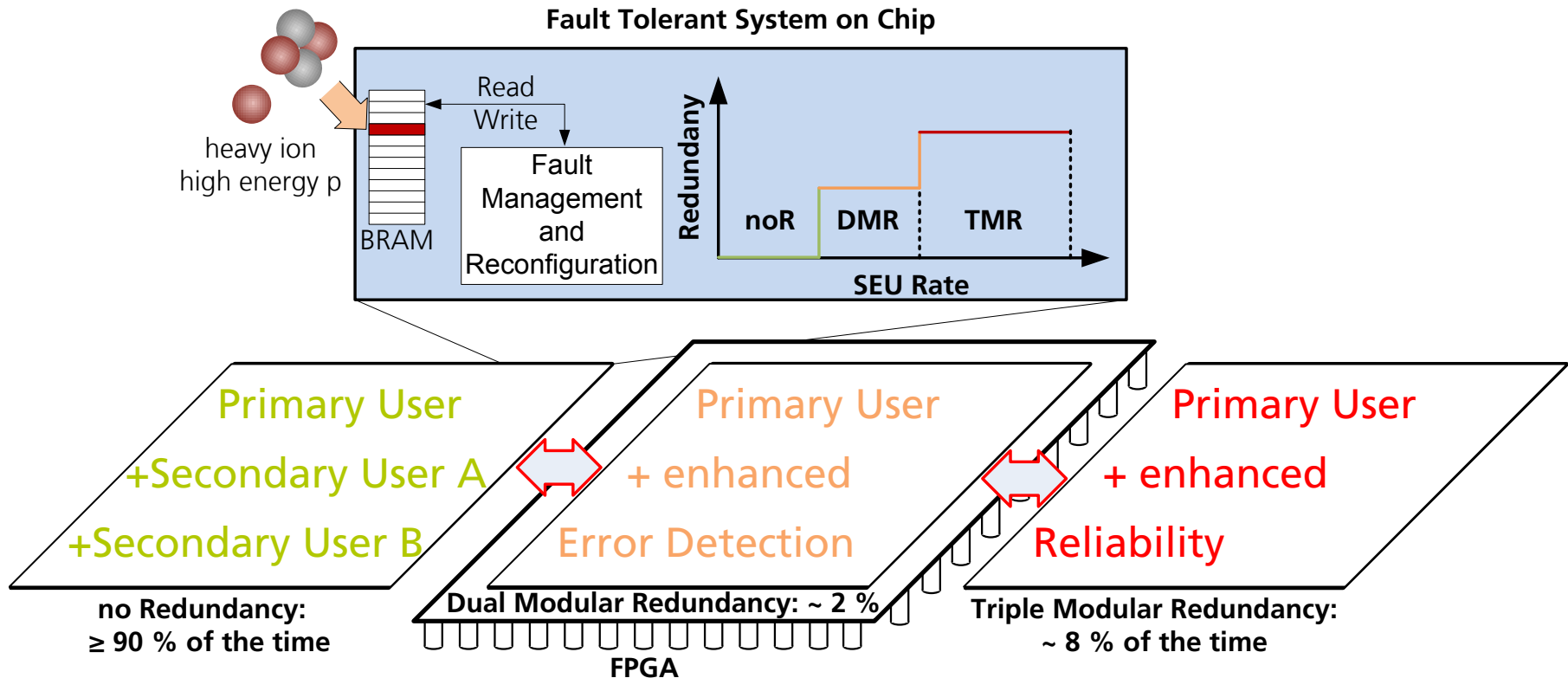Triple Modular Redundancy:
~ 8 % of the time

- **Triplicate** the data **throughput at no flare** condition compared to TMR

- **Decrease the PFH** (probability of failures per hour) **by 20,000 at flare-enhanced** conditions compared with a non-redundant system

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Adaptive Mitigation
Optimal Redundancy at Runtime in Cognitive Radio

Fault Tolerant System on Chip

heavy ion
high energy p

BRAM

Read
Write

Fault
Management
and
Reconfiguration

Redundany

noR DMR TMR

SEU Rate

Primary User
+Secondary User A
+Secondary User B

Primary User
+ enhanced
Error Detection

Primary User
+ enhanced
Reliability

no Redundancy:
≥ 90 % of the time

Dual Modular Redundancy: ~ 2 %

FPGA

Triple Modular Redundancy:
~ 8 % of the time

- **Triplicate** the data **throughput at no flare** condition compared to TMR

- **Decrease the PFH** (probability of failures per hour) **by 20,000 at flare-enhanced** conditions compared with a non-redundant system

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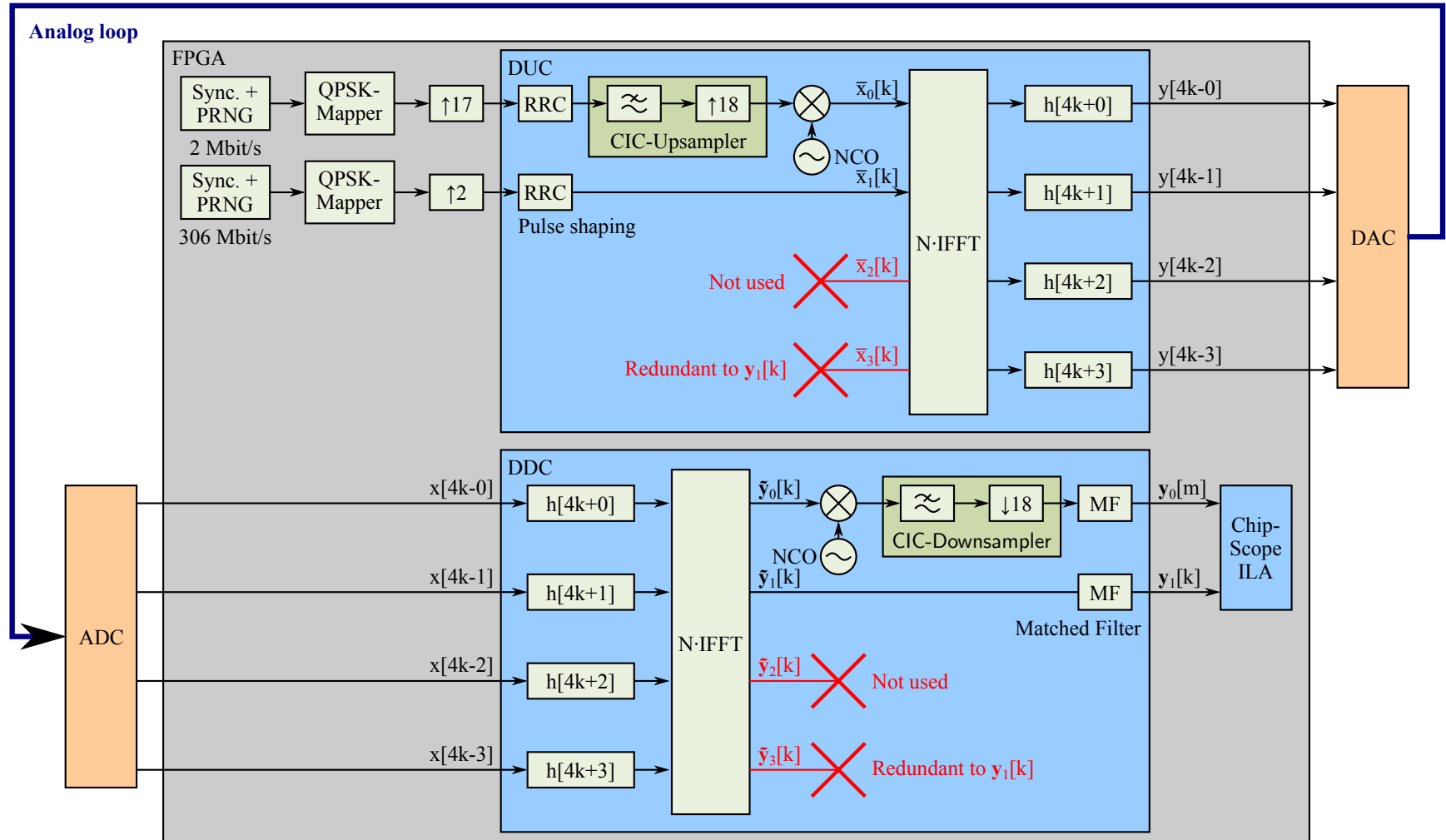HEINRICH HERTZ

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Broadband Processing
System Concept – Second FPGA

- Analog bandwidth BW_A = 450 MHz

    - Goal: Maximum possible bandwidth and one further narrowband

- ADC with data quad-demultiplexing

    - Sampling frequency f_S = 1224 MHz

    - 4 buses with 306 MHz data clock

        - Processing clock on Virtex-5QV f_{Proc} = 306 MHz

- Maximal frequency for Virtex-5QV f_{5QV} = 360 MHz

- Digital Up Converter (DUC)

    - Combines sub-bands, multiplexes buses

- **Digital Down Converter (DDC)**

    - Combines buses, extracts sub-bands

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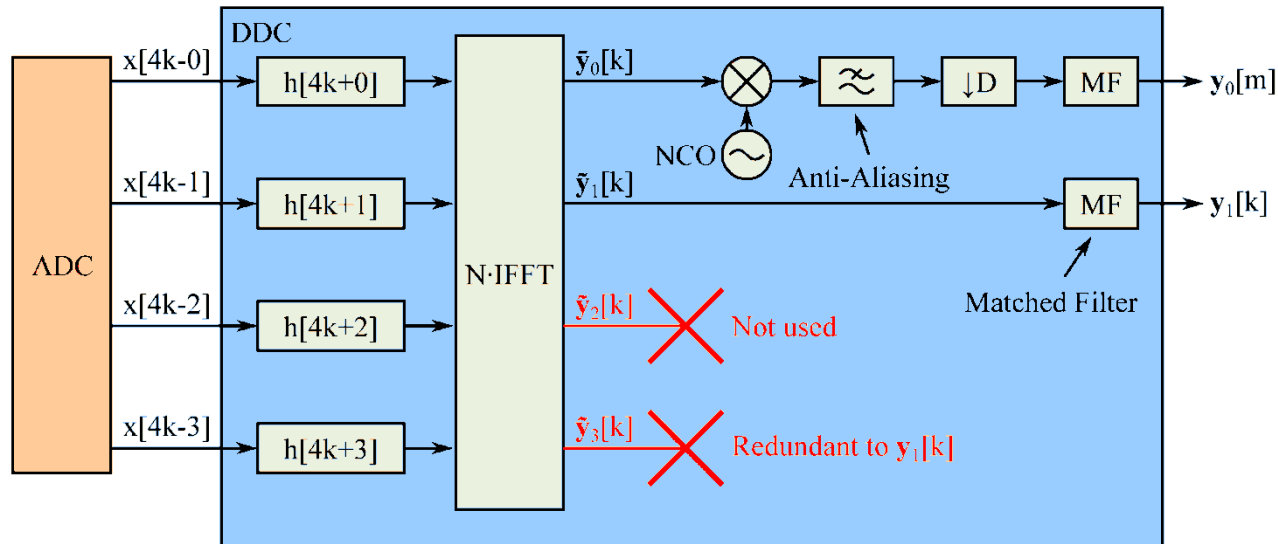
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Broadband Processing
DUC (Digital Up Converter) & DDC (Digital Down Converter)

Broadband Processing [3]
DDC (Digital Down Converter)

- Polyphase filter bank with additional downsampling

  - Channel 0 → signaling (narrowband)

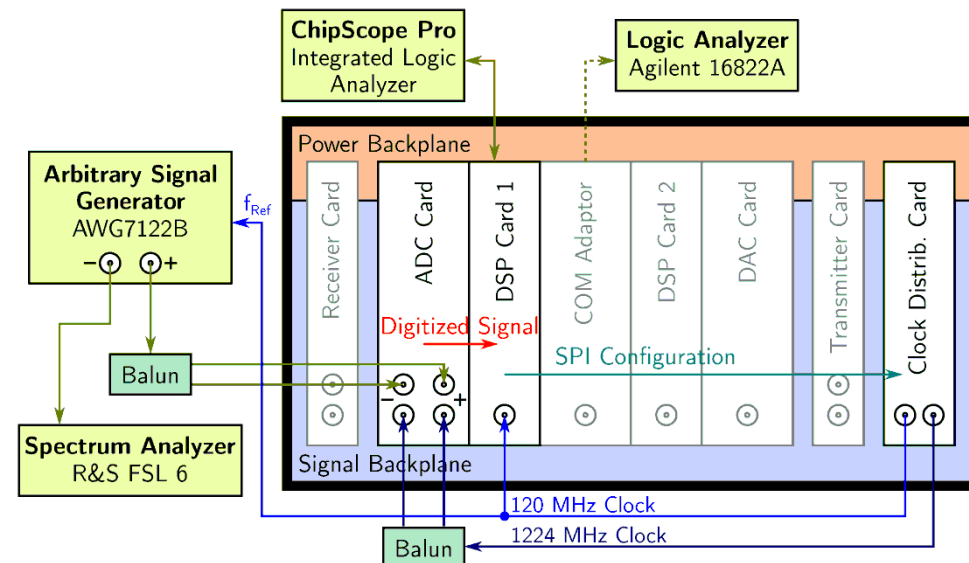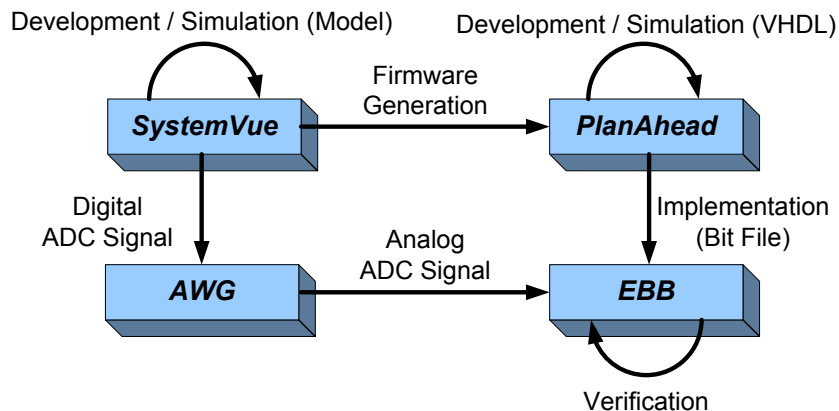 - Channel 1 → maximum possible bandwidth (broadband)

- Design challenge: $f_{5QV} = 360$ MHz vs. $f_{Proc} = 306$ MHz

Broadband Processing
Case Study: Overview

- Implementation of the DDC (System-Vue)

- VHDL simulation (Modelsim)

- Hardware Verification with an *Arbitrary Waveform Generator* (AWG)

  - Oversampling at 18.36 GS/s (max. 24 GS/s)

- Clock,- ADC- and DSP-card
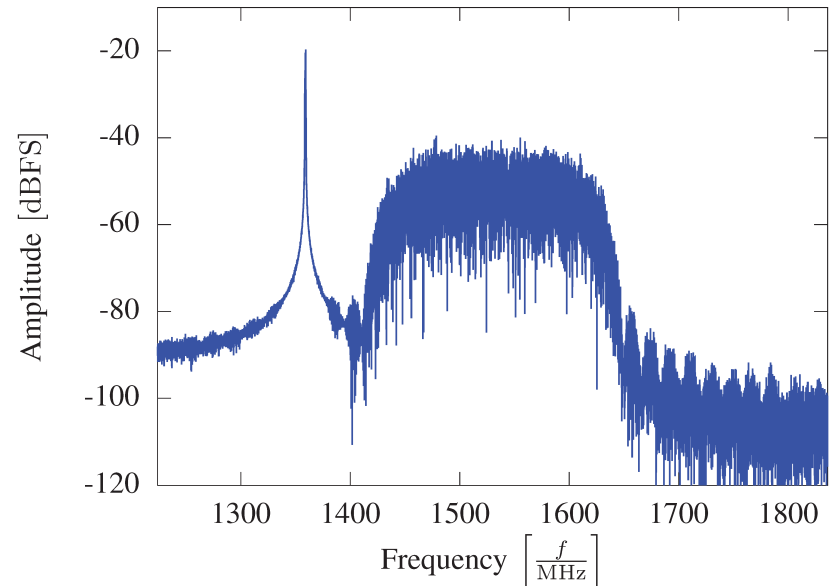
Broadband Processing
Case Study: Results using QPSK on the EBB

- Symbol rates

  - Narrowband channel: 1 MBd (2 Mbit/s , 1.5 MHz, α = 0.5)

  - **Broadband channel:** 153 MBd (306 Mbit/s, 229.5 MHz, α = 0.5)

- ChipScope takes IQ snapshots and Matlab calculates the SNR/EVM

- **Results**

	SNR	EVM
Simulation	21.17 dB	6.71%
Hardware	19.29 dB	9.62%

- Xilinx Timing Score

  - 9378 ps (Virtex5-QV)

QPSK: Quadratur Phase-Shift Keying, α: Roll-off factor, SNR: Signal-to-Noise Ratio, EVM: Error-Vector-Magnitude

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Broadband Processing
Case Study: Resources and SEU Rates

■ Resources

Resource Type	Available	Virtex5-COTS	Virtex5-QV
Flip Flops	81,920	4,538 (5.5 %)	4,555 (5.6 %)
LUTs	81,920	3,152 (3.8 %)	3,171 (3.9 %)
DSP-Slices	320	95 (29.7 %)	95 (29.7 %)
BRAM	298	11 (3.7 %)	11 (3.7 %)
Essent. CfgBits	34,087,072	862,576 (2.5 %)	885,131 (2.6 %)

■ SEU rates

Solar-Minimum	**99.5 h** mean time to upset
Worst-Week	**15 m** mean time to upset
Peak-5-Minutes	**70 s** mean time to upset

$$\mu_{\mathrm{DDC}} = \sum_n \left(\mu_n \cdot \frac{n_{\mathrm{Design}}}{n_{\mathrm{Available}}} \right)$$
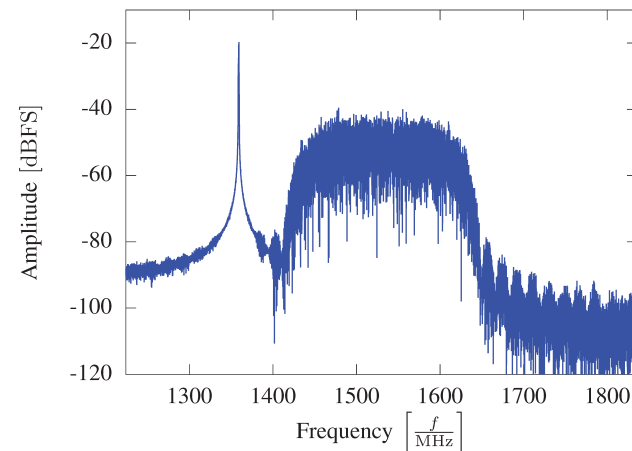
■ → Operation in each solar condition

COTS: Commercial Off-The-Shelf, LUT: Look-Up-Table

Conclusion I

- Heinrich Hertz satellite mission: 15 years in GEO

- Fraunhofer On-Board Processor (FOBP): Based on two Virtex-5QV

  - Up to 450 MHz processing bandwidth

- Initial configuration, start-up and reconfiguration

  - Master-slave negotiation and reconfiguration for experiments

  - Reconfiguration reliability **increases by 12.1 %** ($R_{parallel}$=99.8 %)

- Self-adaptive single event upset (SEU) mitigation

  - **Internal block RAM (BRAM) radiation particle sensor**

  - Triplicate the data throughput → over 90 % of the time (static overhead for fault mngmt.)

  - **Optimal redundancy at runtime** for a **cognitive radio** application

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Conclusion II

- Broadband Processing

  - DDC with polyphase filter bank and additional down converter

  - Case Study → DDC Implementation

    - 306 Mbits/s with QPSK possible (on EBB with an SNR of 19.29 dB)

    - During the Peak-5-Minutes only 70 s mean time to upsets (for DDC)

- Latest publications:

  - [1] Xcell 84:   Ensuring FPGA Reconfiguration in Space

  - [2] FCCM'14: A Self-Adaptive SEU Mitigation System for FPGAs with an Internal Block RAM Radiation Particle Sensor

  - [3] AHS'14:   Broadband FPGA Payload Processing in a Harsh Radiation Environment (upset rate typo in Chapter VI)

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