



Selex ES

A Finmeccanica Company

Wireless Innovation Forum European Conference
November 6th, 2014, Rome (Italy)

Software Defined Radio Workshop



AGENDA

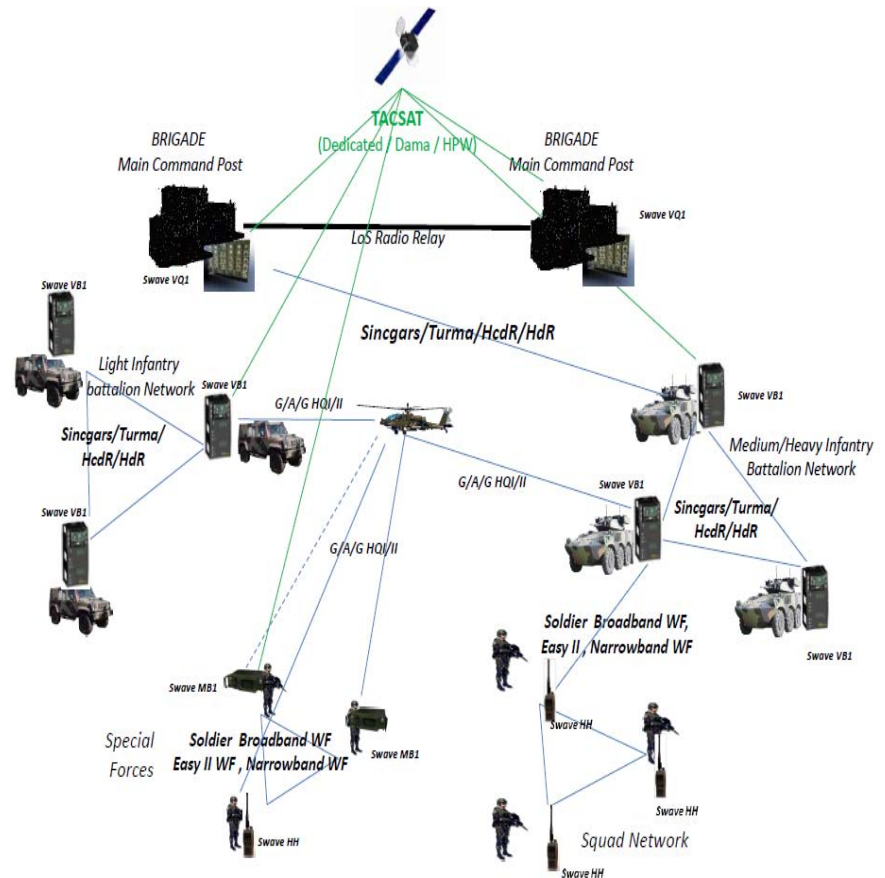
SELEX ES SWave® Family of Software-Defined-Radios for Land Tactical Communications

Design and development of:

- 1. A protection circuit for software-defined-radio front-end**
- 2. A Low IF Receiver architecture**
- 3. A Polar Modulator architecture**

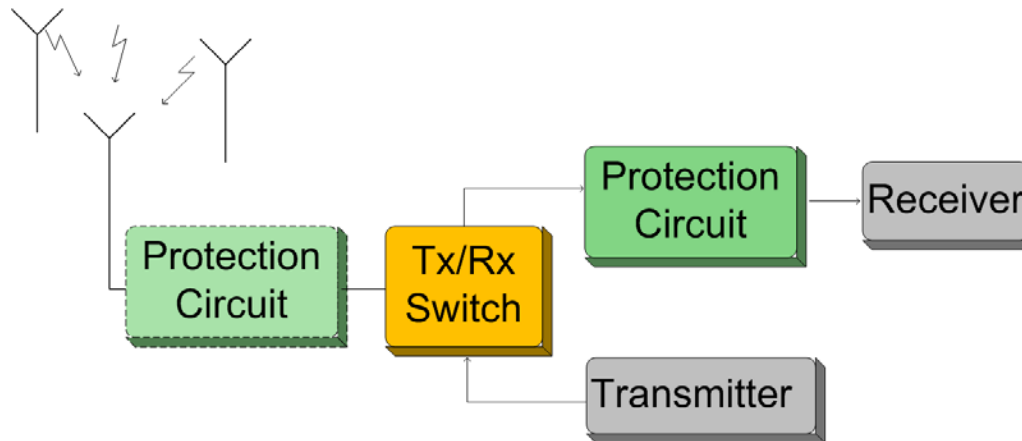
Land Tactical SWave® family

Software-Defined-Radio Products in the military hierarchy



Design & Development of a front-end radio protection circuit

- RF front end protection circuit against antenna received high level signals (wanted and disturbant).



How it works ?

- When the input voltage of the circuitry to be protected tends to exceed a threshold voltage, the protection circuit shunt the current toward the ground.

Design & Development of a front-end radio protection circuit

✶ Which are the literature-based solutions ?

Protection solutions are closely related to operating band of the transceiver.

For transmission that not exceed a hundred of MHz (HF/VHF):

- use of electronic power components (to shunt all the current to ground)
- noise/disturbant and useful signals are full received by the antenna

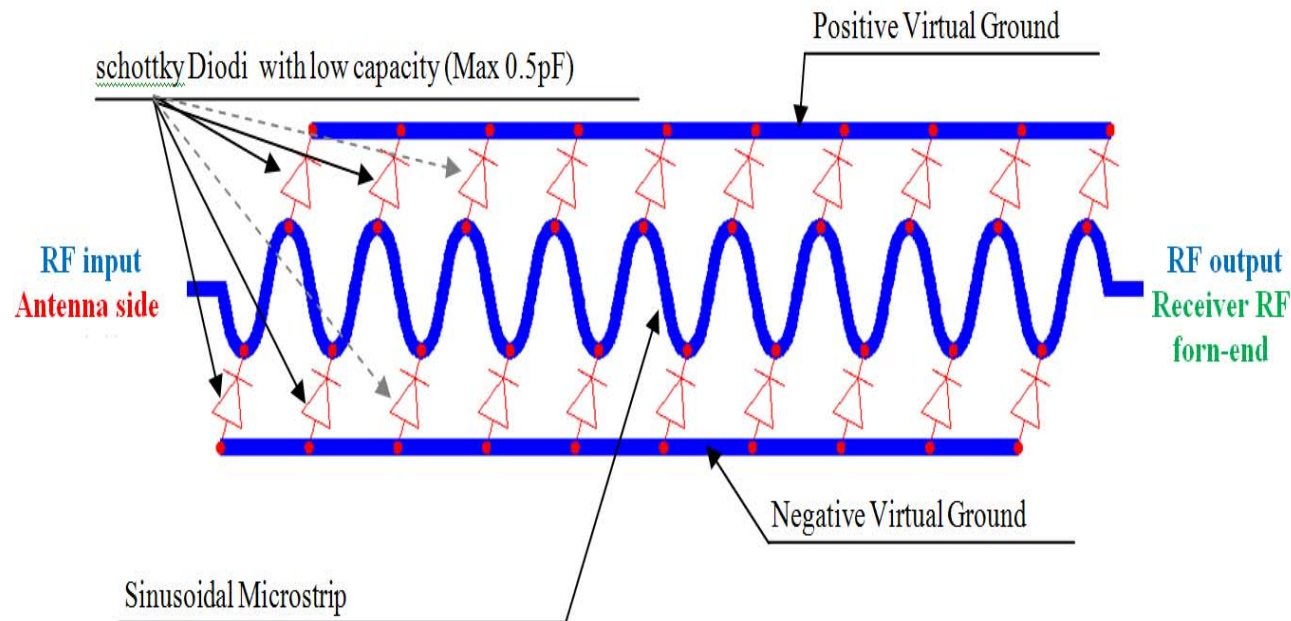
For transmission that exceed a hundred of MHz (UHF):

- Typically, the UHF protection systems envisage the presence of a stub and it's based on the fact that the useful electromagnetic signals and the disturbance have different frequencies. In fact, the stub behaves as a band-pass filter, resonating with high impedance at the band-centre
- antennas are quite selective themselves

Design & Development of a front-end radio protection circuit

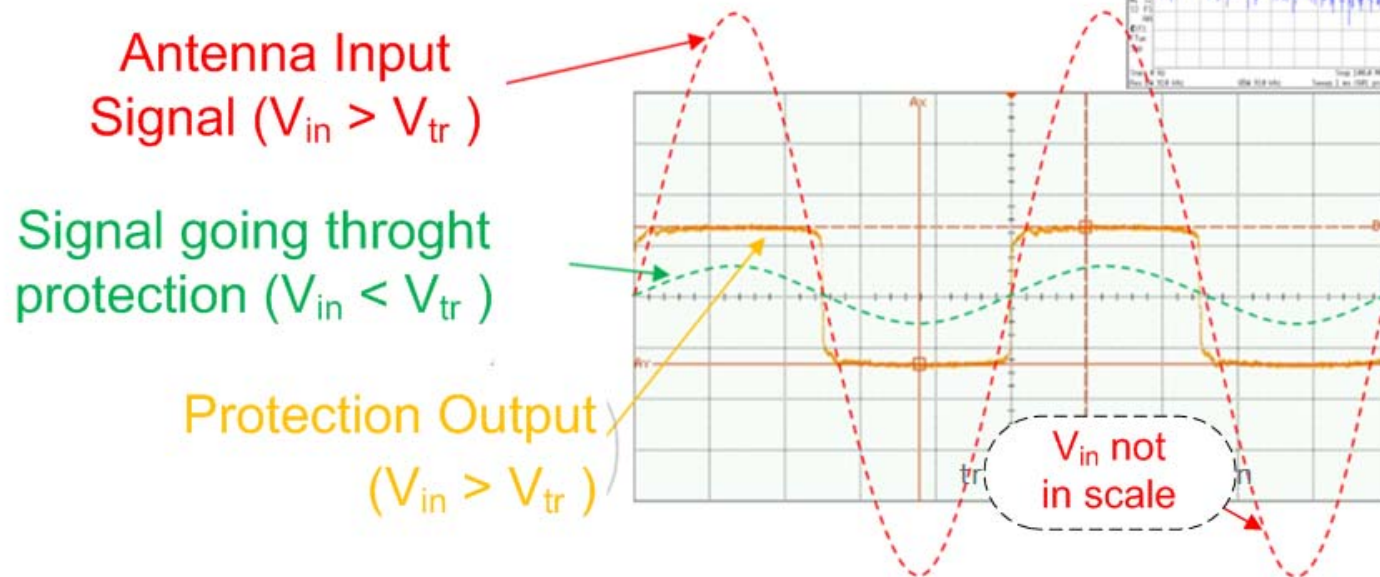
☼ How has it been designed & developed ?

It consists in a sinusoidal microstrip and a set of diodes with the respective anode connected to a corresponding point of maximum of sinusoidal microstrip and positive virtual ground microstrip and an analogue set of diodes connected to a corresponding point of minimum of sinusoidal microstrip and negative virtual ground microstrip.



Design & Development of a front-end radio protection circuit

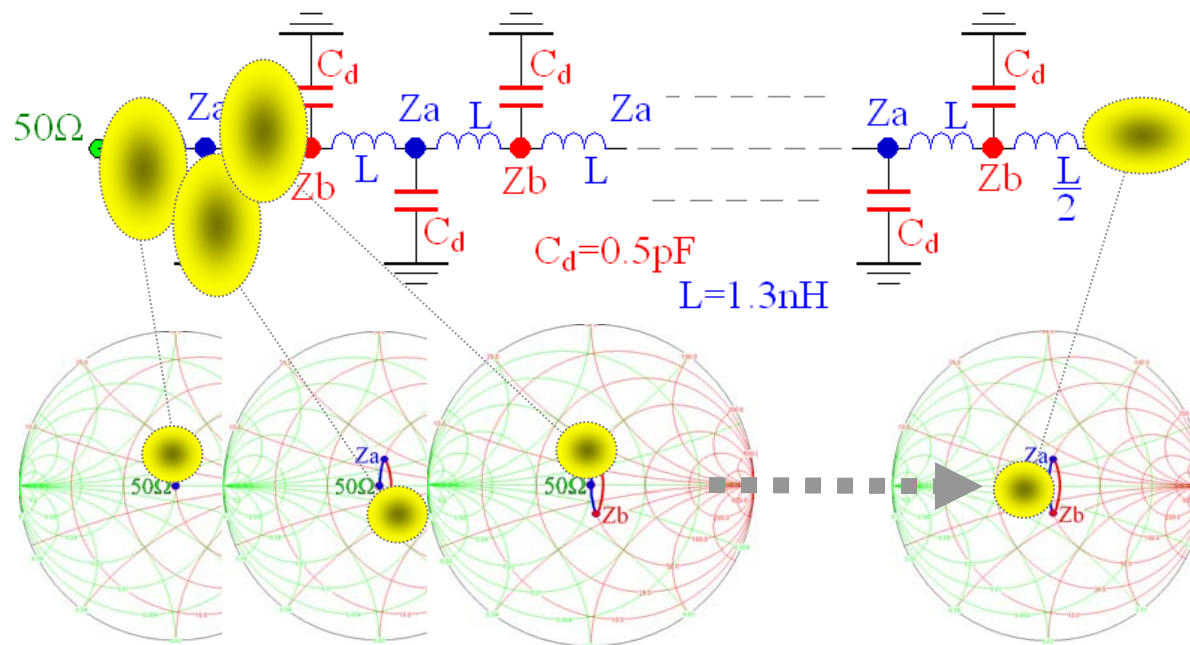
- Power diodes are connected in such a way that, if the input voltage of the circuitry to be protected tends to exceed a threshold voltage, they clamp this input voltage to the threshold voltage (tuned by pos/neg virtual ground lines), and absorb the current that exceeds the allowed maximum current, conveying it to ground.



Design & Development of a front-end radio protection circuit

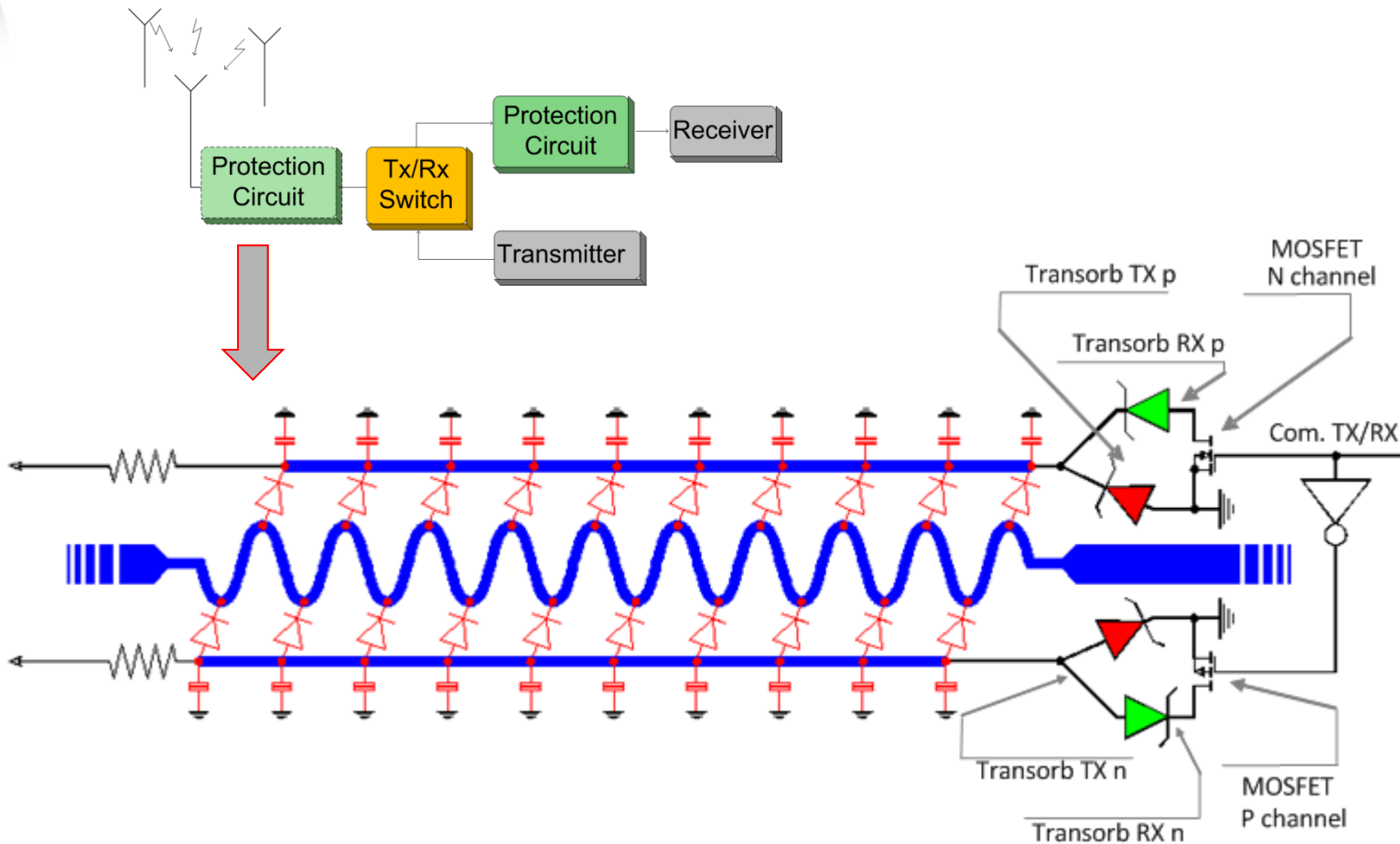
✧ Equivalent Circuit

- A period of the serpentine and a couple of diodes are the elementary element. Geometrical shape and elect. spec. of diodes are used to dimension the protection for higher frequency.
- The number of elementary element allow to shunt the max current related to the lower frequency range.



Design & Development of a front-end radio protection circuit

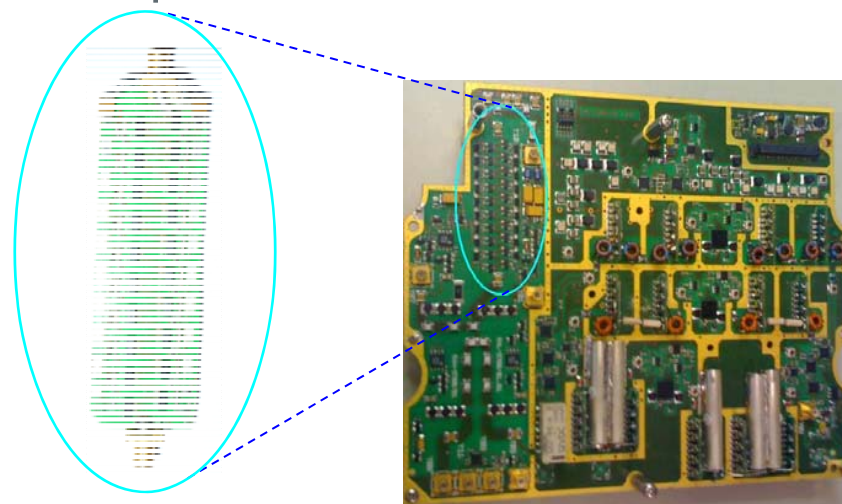
✱ How to protect the transmit stage for low power radio ?



Design & Development of a front-end radio protection circuit

What's the novelty ?

- The protection circuit merges solutions generally adopted in specific freq. range radios in an original and cost-effective solution.
- Thanks to diodes characteristic and shape of the microstrip serpentine, the circuit is easily dimensioned to cope a wide frequency range (30-512 MHz is a typical range for SDR tactical radios) and signal level protection.



Design & Development of a Low IF Receiver Architecture

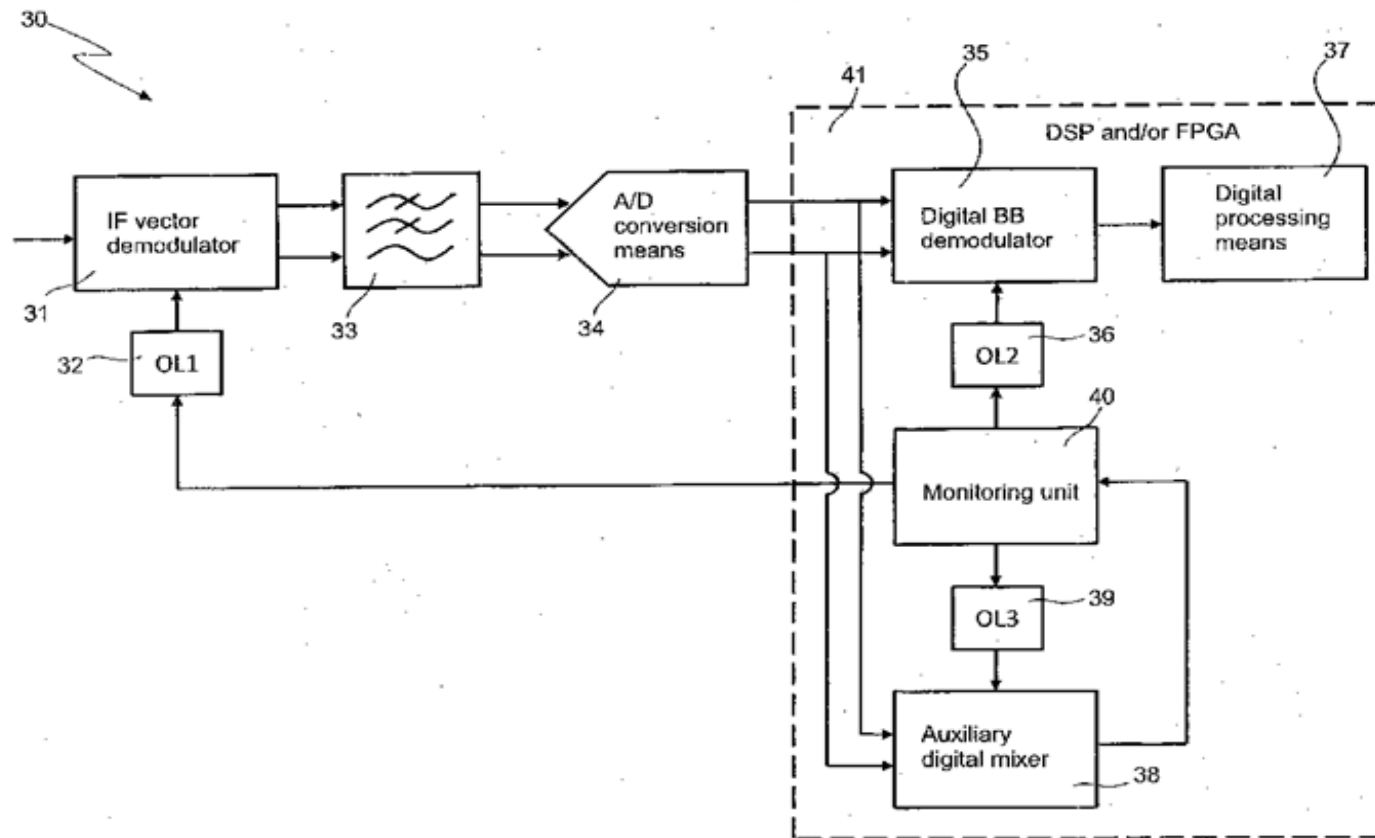
What it is ?

- ✦ IF receiver architecture that is able to solve the image band problem and, in particular, to reject any interfering signals so as to ensure correct demodulation of a received useful signal without having to interrupt the reception service.
- ✦ The architecture is designed to shift a received RF signal to an IF by means of an analog IF mixer that produces corresponding signals I and Q, which are acquired by high sampling frequency A/D conversion means and successively converted from IF to BaseBand in the digital domain by means of a BaseBand digital mixer.

Design & Development of a Low IF Receiver Architecture

How is made ?

- It's a sort of superheterodyne receiver with the IF stage near to DC and dinamically managed.



Design & Development of a Low IF Receiver Architecture

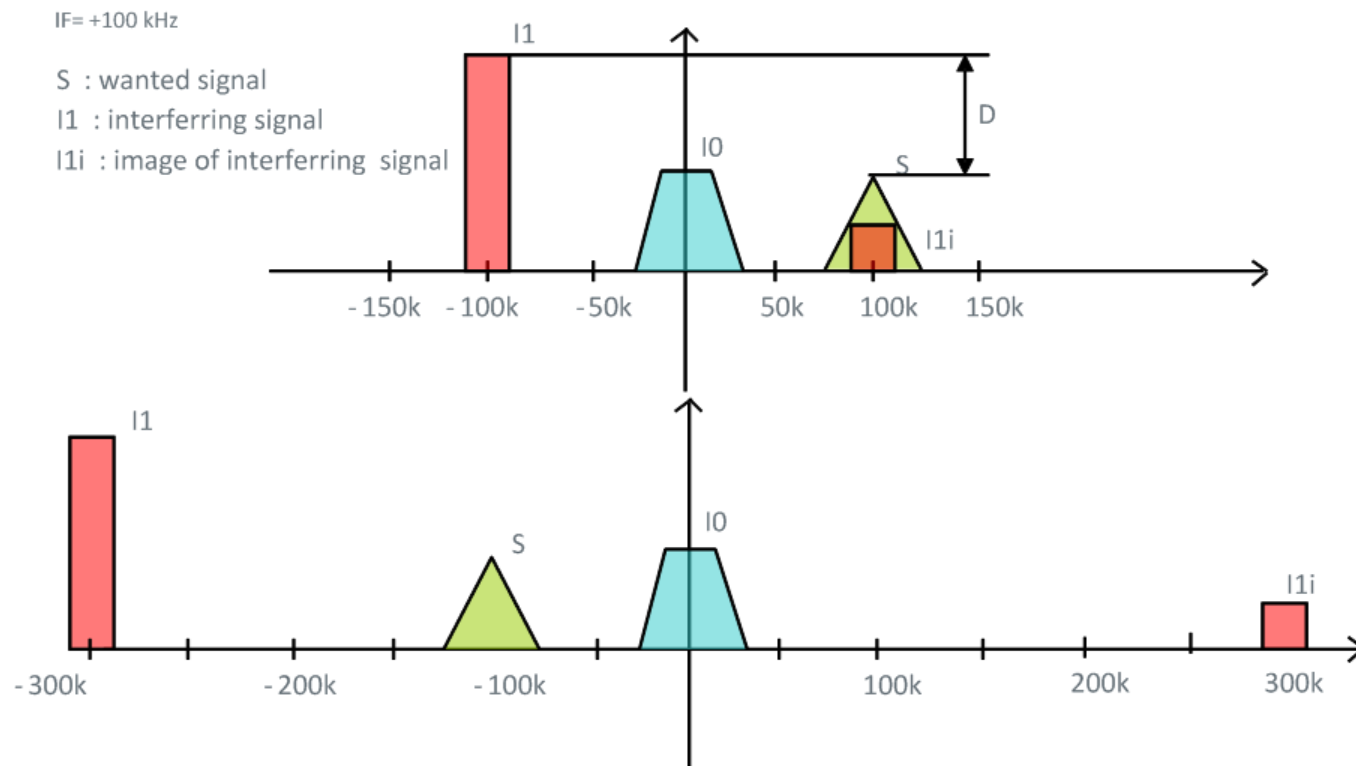
How it works ?

- ✦ The receiver comprises a monitoring branch configured to monitor interference experienced at a plurality of intermediate frequencies usable in reception and select the intermediate reception frequency from the intermediate frequencies usable in reception on the basis of the interference monitoring carried out.
- ✦ The monitoring unit (40) is configured to carry out real-time monitoring of interference experienced at the currently used intermediate reception frequency and also at the other intermediate frequencies usable in reception and change, in real time, the used intermediate reception frequency on the basis of the real-time interference.

Design & Development of a Low IF Receiver Architecture

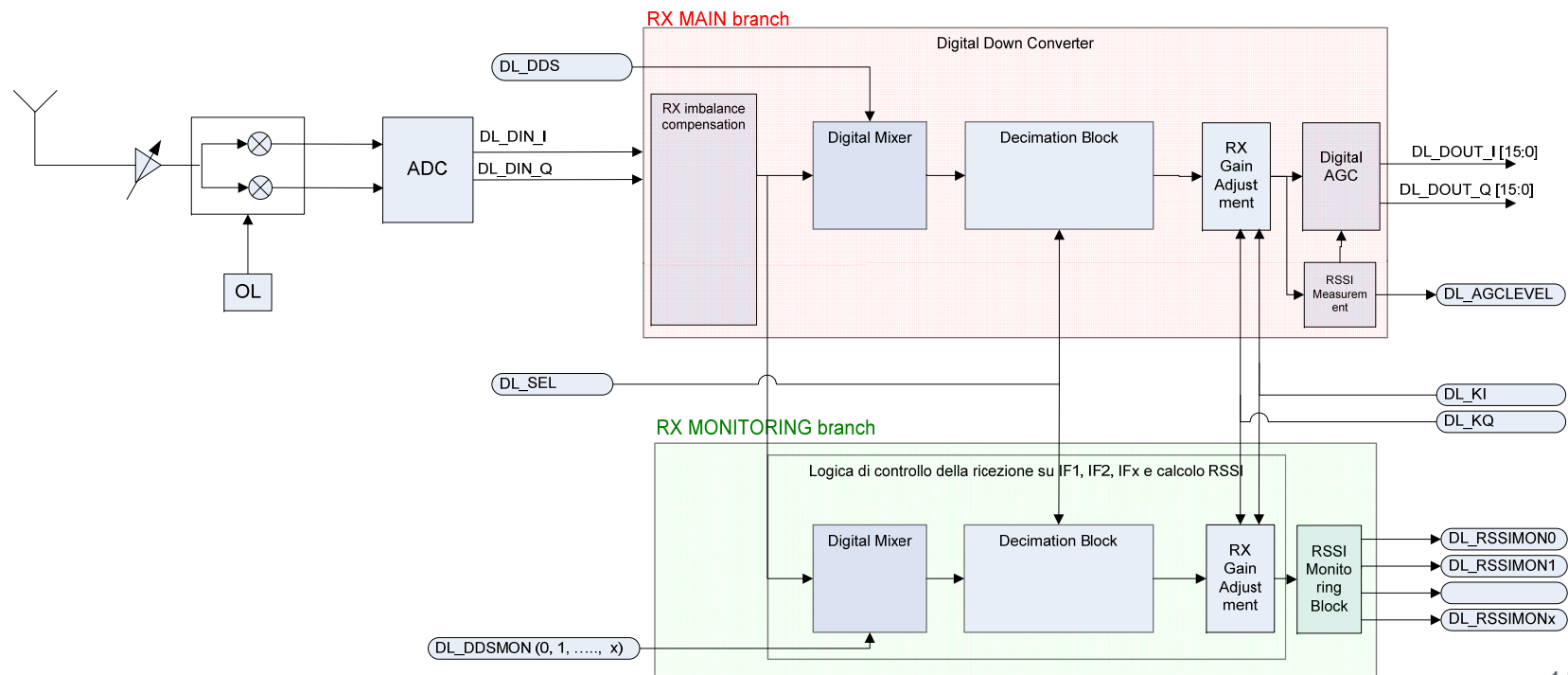
✱ What are the advantages ?

IF value used in reception is chosen dynamically as a function of one or more possible interfering signals and the useful signal band.



Design & Development of a Low IF Receiver Architecture

The monitoring branch keeps updated a table of values of IF and its corresponding quality of reception, with the ability to choose from time to time the best IF value currently available. In this way, interference signals entering the bandwidth of the A/D (typically $\pm 10\text{MHz}$) can be avoided by bringing the desired signal in less or not disturbed frequencies.



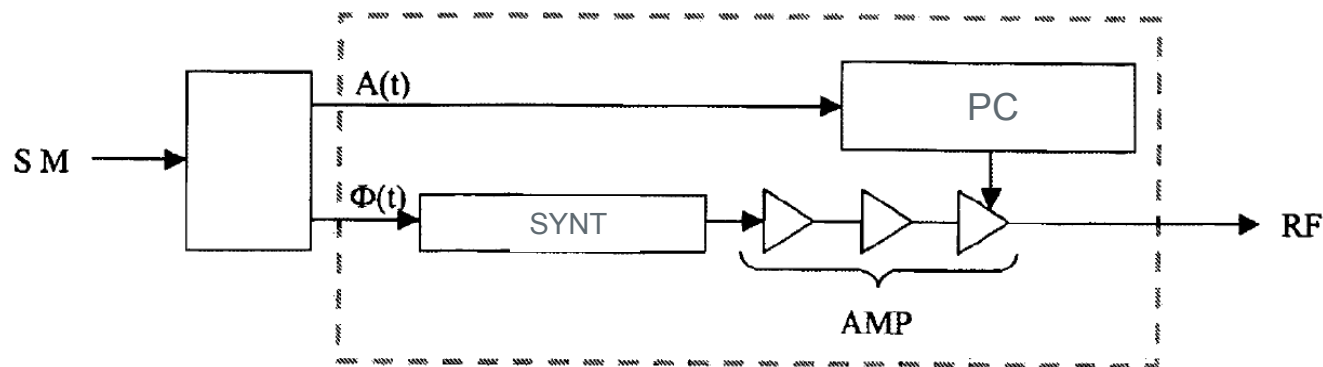
Design & Development of a Low IF Receiver Architecture

- ✦ The Low IF receiver is able to predict the frequency jump to perform if RF conditions arise such that the IF chosen for receiving at the operating frequency must be abandoned. This prediction enables always receiving under the best conditions with respect to radio interference and noise.
- ✦ The proposed architecture could also implement some other modes of reception, including the Zero-IF or the more conventional superheterodyne type, in which the IF assumes relatively high values such as 70/90 MHz.
- ✦ For all these reasons, this implementation of low IF receiver has high resistance to interfering signals and, therefore, high efficiency, high reliability, simplicity and low manufacturing costs, low consumption, signal bandwidth flexibility, ease of use for end users and is suitable for covering wide operating frequency ranges.

Design & Development of a Polar Modulator architecture

What it is ?

- ✦ To produce a radio transmitter capable of performing each type of modulation (analogue and/or digital), the typical approach is to use a low I-Q level (Cartesian) modulator or digital direct conversion architecture followed by class A radiofrequency amplifiers; in this manner, high efficiency is not achieved; indeed the typical efficiency of such a solution is less than 50%.
- ✦ To strongly increase efficiency a polar modulator architecture can be implemented.



Design & Development of a Polar Modulator architecture

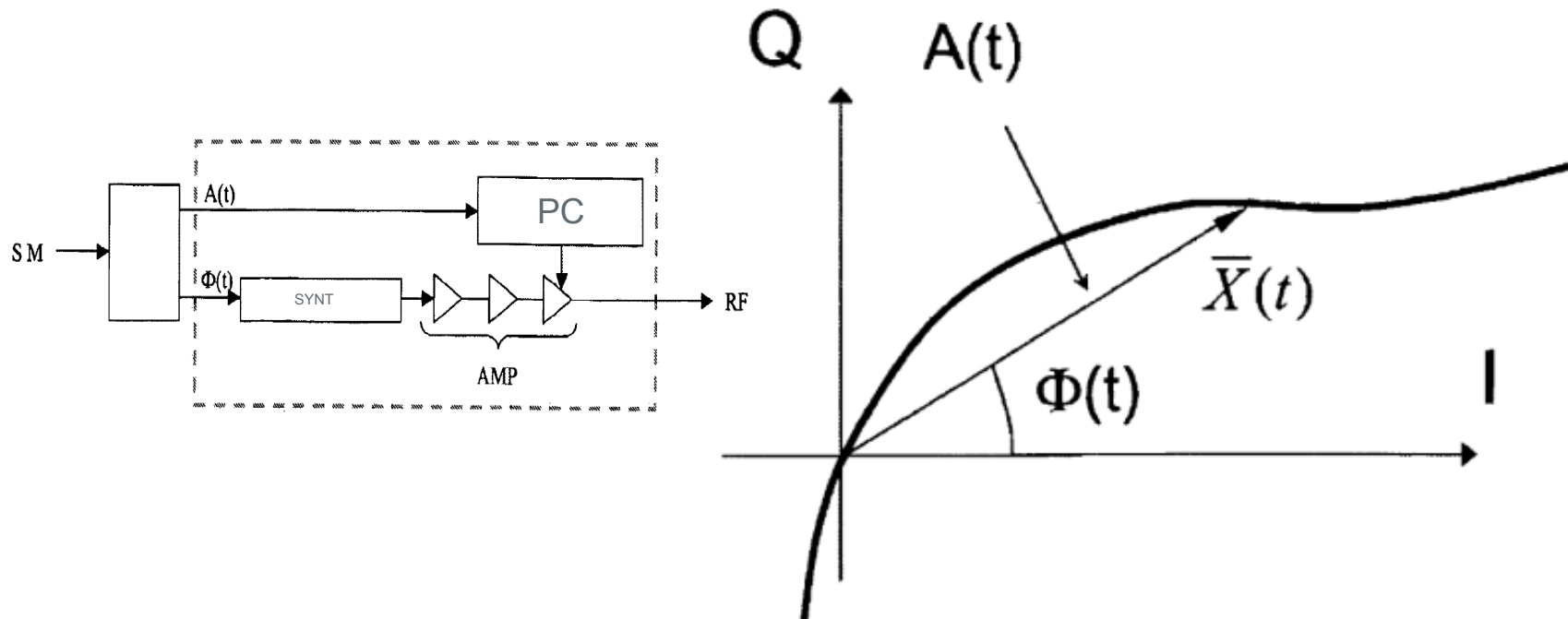
How it is made ?

- ✱ The polar modulator HW architecture is composed mainly by:
 - phase modulation carried out according to a synthesizer (SYNT)
 - amplification of the signal generated by the synthesizer (SYNT) using a chain of radiofrequency power amplifiers AMP in a saturated class (class AB, B, C, D, E or F) to achieve high efficiency at radiofrequency
 - envelope, i.e. amplitude, modulation introduced through a power converter (PC) in the final radio-frequency amplifier stage by varying its supply voltage.

Design & Development of a Polar Modulator architecture

How it works ?

PM receives at its input a modulating signal SM, split up into the amplitude $A(t)$ and the phase $\Phi(t)$ of the modulating signal and which delivers at its output an amplitude-modulated radiofrequency signal RF, i.e. $X(t) = A(t) \cdot \cos(\omega_0 t + \Phi(t))$.



Design & Development of a Polar Modulator architecture

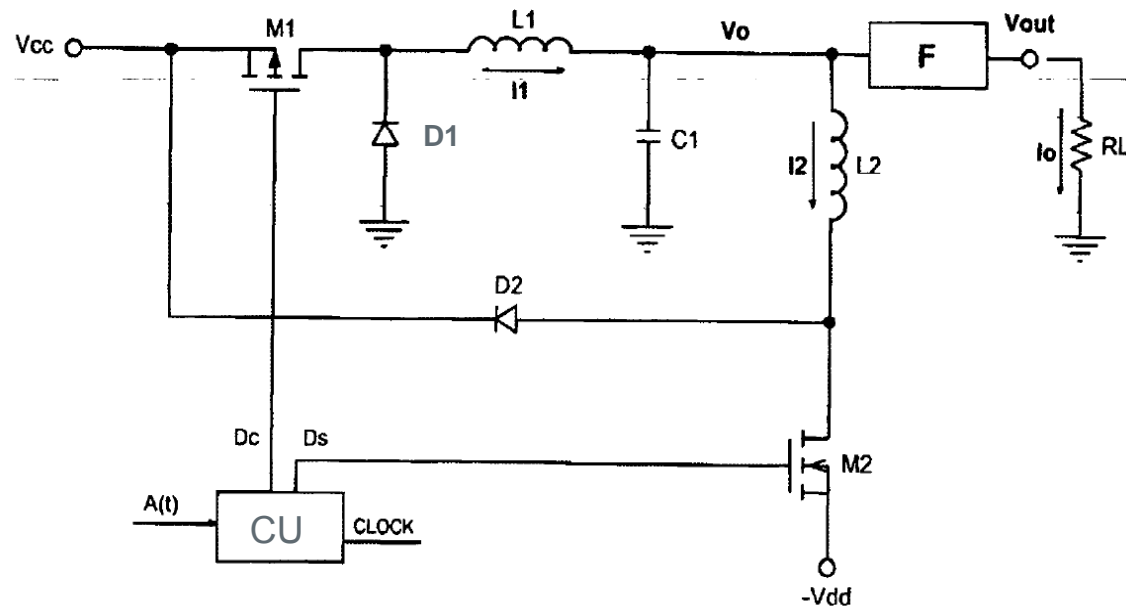
- ✦ The envelope modulator manages almost all the power absorbed by the transmitter; it is therefore important that its efficiency be very high. Furthermore, the envelope modulator must supply, to the final amplifier stage, a variable voltage having the dynamic range set by the modulating signal $A(t)$.
- ✦ Achieving amplitude modulation by varying the supply voltage of the final amplifier stage has been known for at least 70 years, often referred to as "plate modulation".
- ✦ In the last years, the approach proposed in literature applies a step-down regulator (PWM and/or linear) as driving device for the radiofrequency power amplifier in class AB, B, C, D, E or F or other 'saturated' classes, by varying its supply voltage

Design & Development of a Polar Modulator architecture

- ✦ The general aim of the present polar modulator implementation is to eliminate or reduce the drawbacks inherent in the PWM regulator without use of linear regulators achieving a simple and very efficient transmitter stage for tactical SDR radios.
- ✦ One of the innovative aspects of the present implementation is the combining of two different PWM regulators.
- ✦ Two PWM regulators and their switching circuit components M1 and M2 are controlled by an appropriate control unit, indicated CU in Fig. 3, generally hosted in a DSP or FPGA.

Design & Development of a Polar Modulator architecture

- Referring to schematic: the first, made up of an inductor $L1$, a capacitor $C1$, a transistor $M1$ and a diode $D1$, is a step-down regulator and manages the flow of power from the main electrical power source, i.e. the positive voltage source V to the load R_L , assumed to be substantially resistive; the second, made up of an inductor $L2$, a transistor $M2$ and a diode $D2$, is a step-up regulator and provides a fast discharge of the circuit components $L1$ and $C1$, i.e. the two components of the first regulator that store energy.





Thank You

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